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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/008,699	11/08/2001	Tai H. Nguyen	TI-30112	5156

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 11/03/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/008,699	NGUYEN ET AL.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6 and 9-22* is/are rejected.

7)☒ Claim(s) *7 and 8* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07252002*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement (IDS) submitted on July 25, 2002 was filed before the mailing date of the first Office Action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

2. Claims 10 and 12 are objected to because of the following informalities:

- As per claim 10, "... wherein said each clock gate *is* at least one of said plurality of enablement bits..." should be "wherein said each clock gate *receives* at least one of said plurality of enablement bits..." or the like.
- As per claim 12, "... wherein said clock gates each *comprise*..." should be "... wherein said clock gates each *comprises*..."

Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Re Claims 1, 3-5, 14-15 and 17-19

4. Claims 1, 3-5, 14-15 and 17-19 are rejected under 35 U.S.C. 102(e) as being anticipated by Howard et al., US Patent 6711691, hereinafter Howard.

5. In re claim 1, Howard discloses a digital signal processing system [computer system 100], comprising:

- At least one shared component [memory controller/bus manager 112].
- A plurality of processor subsystems [processors a-d 102-108] that share said shared component [fig.1c; processors share memory and bus].
- A clock tree configured to provide a clock signal to said shared component [fig.1c; col.10, ll.53-64; pllc a-d and internal pll for 112 forms clock tree], wherein the clock signal is disabled only if each of the plurality of processor subsystems disables the shared component [col.14, l.45 – col.15, l.39; deactivate the processors deactivates the shared component with all clocks eventually shut down].

6. As to claim 3, Howard discloses the system wherein the shared component comprises a shared program memory [DRAM 114] [fig.1c; col.7, ll.10-34].

7. As to claim 4, Howard discloses the system wherein the shared component comprises an external input/output port (XPORT) arbiter [i/o interrupt controller 116] [fig.1c; col.7, ll.35-67].

8. As to claim 5, Howard discloses the system wherein each of the plurality of processor subsystem includes a processor core having an external input/output port (XPORT) interface coupled to an external input/output port (XPORT) [fig.1c; col.7, ll.35-52; inherently, an interface with an associated port in the broadest interpretation is needed for each of the processors to receive interrupts a-d].

9. In re claim 14, Howard discloses a method of providing a clock signal to a shared component [memory controller/bus manager 112] shared by a plurality of subsystems [processors a-d 102-108], wherein the method comprises:

- Generating a clock signal [col.10, ll.53-64].
- Passing the clock signal to the shared component only if at least one of the subsystems has not de-asserted a shared component enablement bit [inverse of QREQ] [col.6, l.55 – col.7, l.9; col.14, l.45 – col.15, l.39; asserting QREQ is tantamount to de-asserting an enablement bit; if at least one QREQ is not asserted, then the clock signal to the shared component would still be active].

10. As to claim 15, Howard discloses the method comprising blocking the clock signal to the shared component [memory controller/bus manager 112] only if each of the plurality of subsystems [processors a-d 102-108] has de-asserted a corresponding shared component enablement bit [asserted QREQ] [col.6, l.55 – col.7, l.9; col.14, l.45 – col.15, l.39; the clock signal is stopped when all QREQs have been asserted].

11. As to claim 17, Howard discloses the method wherein the shared component comprises a shared program memory [DRAM 114] [fig.1c; col.7, ll.10-34].

12. As to claim 18, Howard discloses the method wherein the shared component comprises an external input/output port arbiter [i/o interrupt controller 116] [fig.1c; col.7, ll.35-67].

13. In re claim 19, Howard discloses a digital signal processing system [computer system 100] that comprises:

- An external input/output port (XPORT) [col.7, ll.35-52; ports to accept incoming interrupts].

- An external input/output port (XPORT) arbiter [i/o interrupt controller 116].
- A plurality of processor cores [processor 102-108] configured to access the XPORT wherein each of the plurality of processor cores includes an XPORT interface [inherently, an interface with an associated port in the broadest interpretation is needed for each of the processors to receive interrupts a-d] coupled to the XPORT arbiter [fig.1c; col.7, ll.35-67].
- A clock tree [fig.1c; col.10, ll.53-64; pllc a-d and internal pll for 112 forms clock tree] configured to provide a clock signal to the XPORT arbiter and the XPORT interfaces, wherein the clock tree is configured to disable the clock signal if each of the plurality of processor cores de-asserts a respective peripheral enablement bit [inverse of QREQ] [col.6, l.55 – col.7, l.9; col.14, l.45 – col.15, l.39; asserting QREQ is tantamount to de-asserting an enablement bit; if at least one QREQ is not asserted, then the clock signal to the shared component would still be active].

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Re Claims 2 and 16

15. Claims 2 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard as applied to claim 1 above, and further in view of Hathaway, US Patent 6536024.

16. Howard discloses each and every limitation of the claim as discussed above in reference to claim 1. Howard did not discuss the integration of the various components on a single chip.

17. Hathaway discloses a system [integrated circuit] wherein the plurality of processor subsystems [logic circuits], the shared component [latches, gates, etc.], and the clock tree are fabricated on a single chip [integrated circuit chip] [col.1, l.14 – col.2, l.27].

18. It would have been obvious to one of ordinary skill in the art, having the teachings of Howard and Hathaway before him at the time the invention was made, to integrate the components disclosed by Howard on a single chip as taught by Hathway as the integrated circuit chip taught by Hathaway is a well known entity for integrating the various components of Howard. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to integrate components on a single chip and be more energy efficient [Hathaway: col.1, ll.6-56].

Re Claims 6, 9-10 and 22

19. Claims 6, 9-10, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard as applied to claim 4 above, and further in view of Smith, US Patent 5677849.

20. In re claim 6, Howard discloses each and every limitation of the claim as discussed above in reference to claim 4. In particular, Howard discloses the system wherein the clock tree supplies a corresponding processor clock signal [pllc a-d] to each of the processor cores [fig.1c; col.10, ll.53-64]. Howard did not discuss the details of separately and independently disabling the processor cores by suspension of the corresponding processor clock signal.

21. Smith discloses a system [integrated circuit] wherein a clock tree [fig.1] is configured to separately and independently disable the processor cores [functional blocks] by suspension of the

corresponding processor clock signal [start_clock at high level] from the clock tree [col.2, l.51 – col.3, l.12].

22. It would have been obvious to one of ordinary skill in the art, having the teachings of Howard and Smith before him at the time the invention was made, to modify the system taught by Howard to include the teachings of Smith, in order to obtain the system wherein the clock tree supplies a corresponding processor clock signal to each of the processor cores, and wherein the clock tree is configured to separately and independently disable the processor cores by suspension of the corresponding processor clock signal from the clock tree. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to conserve power by selectively gating clock signals [Smith: col.1, l.8 – col.2, l.9].

23. As to claims 9, Smith discloses the system wherein the clock tree includes a register [flip flops 23-26 form register] having a plurality of enablement bits [output of Q], each of said enablement bits configured to enable a corresponding one of a plurality of clock signals [clk_out 11-14] when asserted, wherein said plurality of clock signals are coupled to a corresponding plurality of processor subsystems [functional blocks] [fig.1; col.3, l.61 – col.4, l.34].

24. As to claim 10, Smith discloses the system wherein the clock tree includes a clock gate [nand 27-30] for each of the plurality of clock signals, wherein said each clock gate receives at least one of said plurality of enablement bit [output of Q] from said register [col.3, l.61 – col.4, l.34].

25. As to claim 22, Smith discloses the system wherein the clock tree provides processor [functional blocks] clock signals distinct from the clock signal to the other functional blocks

[XPORT arbiter] that are configured to be independently blocked and passed [col.2, l.51 – col.3, l.12].

Re Claims 11-13

26. Claim 11-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard and Smith as applied to claim 10 above, and further in view of Barlow et al., US Patent 6311263, hereinafter Barlow.

27. In re claim 11, Howard and Smith disclose each and every limitation of the claim as discussed above in reference to claim 10. Howard and Smith did not discuss the logic gate.

28. Barlow discloses the system [integrated circuit] wherein the clock tree further includes a logic gate [OR gate 802] coupled to each of the shared component enablement bits [cen1-2] and to one of said clock gates [812, 800], wherein the logic gate is configured to assert a gate signal [cen] to said one of said clock gates for the shared component clock [pclk] if at least one shared component enablement bit is asserted [col.19, l.20 – col.20, l.17; cen1-2 bits are ORed and gate signal cen is asserted only if at least one of cen1-2 is asserted].

29. It would have been obvious to one of ordinary skill in the art, having the teachings of Barlow, Howard and Smith before him at the time the invention was made, to modify the system taught by Howard and Smith to include the teachings of Barlow, in order to obtain the system wherein the clock tree includes a logic gate coupled to each of the shared component enablement bits and to one of said clock gates, wherein the logic gate is configured to assert a gate signal to said one of said clock gates for the shared component clock if at least one shared component enablement bit is asserted. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to implement in logic design the clock tree wherein the

clock signal is disabled only if each of the plurality of processor subsystems disables the shared component [Barlow: col.19, l.20 – col.20, l.17; none of the cen1-2 bits can be asserted in order for cen to be activated].

30. As to claim 12, Smith discloses the system wherein said clock gates each comprises gated inverting buffers [36-39] and Barlow discloses said logic gates comprise logical OR gates [802].

31. As to claim 13, Barlow discloses the system wherein said logic gates de-assert the gate signal [cen] to the corresponding clock gate if none of the shared component enablement bits [cen1-2] are asserted [Barlow: col.19, l.20 – col.20, l.17; none of the cen1-2 bits can be asserted in order for cen to be activated].

Re Claim 20-21

32. Claims 20-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Howard as applied to claim 19 above, and further in view of Barlow.

33. In re claim 20, Howard discloses each and every limitation of the claim as discussed above in reference to claim 19. Howard did not discuss the details of the clock tree.

34. Barlow discloses the system that includes a register [804, 806] having the respective enablement bits [cen1-2], wherein a logic gate [800, 802, 812] coupled to each of the respective enablement bits and configured to assert a gate signal [cen] only if at least one shared component enablement bit is asserted [col.19, l.20 – col.20, l.17; cen1-2 bits are ORed and gate signal cen is asserted only if at least one of cen1-2 is asserted].

35. It would have been obvious to one of ordinary skill in the art, having the teachings of Barlow and Howard before him at the time the invention was made, to modify the system taught by Howard to include the teachings of Barlow, in order to obtain the system wherein the clock

tree includes a register having said respective enablement bits, wherein the clock tree further includes a logic gate coupled to each of the respective enablement bits and configured to assert a gate signal only if at least one shared component enablement bit is asserted. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to implement in logic design the clock tree wherein the clock signal is disabled only if each of the plurality of processors de-asserts the respective enablement bits [Barlow: col.19, l.20 – col.20, l.17; none of the cen1-2 bits can be asserted in order for cen to be activated].

36. As to claim 21, Barlow discloses the system that includes a clock gate [808, 810] coupled to the logic gate [800, 802, 812] to receive the gate signal [cen], wherein the logic gate is configured to block the clock signal only if the gate signal is de-asserted [col.19, l.20 – col.20, l.17; cen is ANDed with clock signal which is blocked if cen is de-asserted].

Allowable Subject Matter

37. Claims 7-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

38. The following is a statement of reasons for the indication of allowable subject matter: the claims are allowable because none of the references cited, either alone or in combination discloses or renders obvious a system with the limitations of claim 7 and the associated base claim and the intervening claims.

Conclusion

39. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The additionally cited US patent documents describe various methods and systems related to clocking and multi-processors with shared resources.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
October 21, 2004

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